3.	a)	With the neat construction diagrams, explain the drain characteristics of n-channel JFET.	6	L2	2	1
	b)	For a Junction Field Effect Transistor (JFET), the I_{DSS} = 6mA, V_p = −4.5V. Determine the drain current I_D for the following cases: i) V_{GS} = −2V ii) V_{GS} = −4V.	6	L3	2	1
	c)	Explain the working of a CMOS inverter with a neat circuit diagram.	4	L2	2	1

Unit – II

4.	a)	With the help of a neat circuit diagram, derive the expression for output voltage of an inverting amplifier circuit using Op-amp. Draw the input and output waveforms considering the input voltage of 2V peak and a gain of 4. Assume the V^+ and V^- as ±12V.	6	L2	3	1
	b)	Design a summing amplifier using Op-amp, to get an output voltage of $V_o = -(3V_1 + 4V_2 + 5V_3)$, assuming a feedback resistor of 120KΩ. Draw the circuit.	6	L3	3	1
	c)	Draw the equivalent circuit of an Op-Amp and write the significance of each parameter in it.	4	L1	3	1
5.	a)	With the help of a neat circuit diagram, derive the expression for the output voltage of an integrator circuit using Op-amp.	6	L2	3	1
	b)	Draw the circuit of a IC 555 timer as an oscillator in astable mode. For an IC 555 based oscillator in astable mode, operating at a duty cycle of 75%, with frequency of operation 1kHz, the values of R_2 = 3.6kΩ and C = 0.1μF. Calculate the value of the resistor R_1.	6	L3	3	1
	c)	An amplifier has an open loop voltage gain of 1000. If the feedback factor is 10%, find the closed loop voltage gain.	4	L3	4	1
6.	a)	State Barkhausen's criterion for generating sustained oscillations. Derive the conditions with the help of an oscillator block diagram.	6	L2	4	1
	b)	With a neat circuit diagram, explain the operation of a RC phase shift oscillator. Analyse the role of RC components as feedback network.	6	L2	4	1
	c)	In a Colpitts oscillator, C_1 = 100pF; C_2 = 260pF. Find the value of L if the frequency of oscillation is 40 kHz.	4	L3	4	1

Unit – III

7.	a)	What is meant by modulation in communication system? Write the needs for modulation.	6	L2	5	1
	b)	Explain the following concepts of a cellular system: i) Frequency reuse' ii) Capacity of a cluster.	6	L2	5	1
	c)	Explain different control and voice channels available between a mobile unit and base station for the initiation of a call in a cellular system.	4	L2	5	1
8.	a)	With a neat diagram, explain the various elements of an Embedded system.	6	L2	5	1
	b)	Differentiate between Microprocessor and Microcontroller.	6	L2	5	1
	c)	Discuss the optocoupler with a diagram. Diagrammatically show the usage of optocoupler.	4	L2	5	1

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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13. **In Colpitts' oscillator, the components used in the feedback network are**
A) 2L and 1C B) 2C and 1L
C) 2R and 2C D) 2L and 2C

14. **With a resistance value of R=1kΩ in a feedback network of RC oscillator, frequency of oscillations generated is 5 kHz. The value of the capacitor C is**
A) 0.129 μF B) 0.0219 μF
C) 129 μF D) 0.0129 μF

15. **Gain with negative feedback is given by $A_f = \frac{A}{1+A\beta}$. The closed loop gain is**
A) A_f B) A
C) β C) None of these

16. **An amplifier has an open loop voltage gain of 1000. If 10% negative voltage series feedback is used, then the closed loop gain is**
A) 99.9 B) 9.9
C) 0.9 D) 990

17. **Which of the following statements are true for von Neumann architecture?**
A) Separate bus between the program memory and data memory B) External bus for program memory and data memory
C) External bus for data memory only D) Shared bus between the program memory and data memory

18. **Harvard architecture has _____**
A) Dedicated buses for data and program memory B) Pipeline technique
C) Complex architecture D) All of these

19. **The unit used for measuring message or information is**
A) Hertz B) Ohms
C) Bits per second D) Meter per second

20. **The inherent interference resistance property between wireless cellular channels is observed in**
A) Frequency Division Multiple Access B) Time Division Multiple Access
C) Code Division Multiple Access D) Space Division Multiple Access

PART - B: DESCRIPTIVE ANSWER QUESTIONS

Unit – I

		Marks	BT*	CO*	PO*
1. a)	With a neat circuit diagram, explain the principle of operation of a full wave bridge rectifier. Draw the relevant waveforms.	6	L2	1	1
b)	Define efficiency and ripple factor of a rectifier. Deduce the maximum values of both parameters for a half wave rectifier.	6	L2	1	1
c)	A 5V regulated power supply is required to produce from a 12V direct current (DC) power supply input source. The maximum power rating Pz of the Zener diode is 2W. Calculate: i) The maximum current following through the Zener diode, ii) The minimum value of the series resistor, Rs, iii) The load current I_L, if a load resistor of 1kΩ is connected across the Zener diode, iv) The Zener current I_z at full load.	4	L3	1	1
2. a)	Explain D.C. load line analysis of a Bipolar Junction Transistor (BJT) in Common Emitter (CE) configuration.	6	L2	2	1
b)	Calculate α and β for a transistor with collector current of 1 mA, base current of 25 μA. Determine the new value of base current to give a collector current of 5 mA.	6	L3	2	1
c)	With a neat circuit diagram, explain how BJT can be made to operate as a switch.	4	L2	2	1

NMAM INSTITUTE OF TECHNOLOGY, NITTE

Off-Campus Centre of Nitte (Deemed to be University)

First Semester B.Tech. (CBCS) Degree Examinations

December 2022

EC1001-1 – BASIC ELECTRONICS

Duration: 3 Hours | Max. Marks:100

Note:

*1) Part – A: Multiple Choice Questions: Answer all **Twenty** questions in the **OMR Sheet** provided. Each question carries equal marks.*

*Part – B: Descriptive Answer type Questions: Answer **Five full** questions choosing **Two full** questions from **Unit – I & Unit – II each** and **One full** question from **Unit – III.***

2) Assume missing data suitably.

PART - A: MULTIPLE CHOICE QUESTIONS — 20 Marks

1. **The voltage at which forward current through the diode starts increasing rapidly is called as**
   A) Cut in voltage B) Breakdown voltage
   C) Saturation voltage D) Cut off voltage
2. **Smaller the ripple factor, the output will have higher components of**
   A) AC B) DC
   C) spike D) pulse
3. **The efficiency of half wave rectifier is about**
   A) 0.46% B) 1.21%
   C) 81.2% D) 40.6%
4. **In a bipolar junction transistor the collector current is controlled by**
   A) Collector voltage B) Collector resistance
   C) Base current D) None of these
5. **If a 2 mV input signal produces a 2V output signal, what is the voltage gain?**
   A) 1000 B) 0.004
   C) 100 D) 0.001
6. **Total emitter current in BJT is**
   A) $I_C + I_{CBO}$ B) $I_B + I_C$
   C) $I_C + I_E$ D) $I_B - I_C$
7. **Which is not a MOSFET terminal?**
   A) Base B) Drain
   C) Source D) Gate
8. **JFET is considered as a voltage controlled device because _____.**
   A) Gate current is controlled by drain voltage B) Gate current is controlled by source voltage
   C) Drain current is controlled by gate voltage D) Drain current is controlled by source voltage
9. **Which of the following electrical characteristics is not exhibited by an ideal op-amp?**
   A) Infinite output resistance B) Infinite bandwidth
   C) Infinite voltage gain D) Infinite slew rate
10. **An integrator circuit using an Op Amp has ..... in its feedback path**
    A) Resistor B) Inductor
    C) Capacitor D) Diode
11. **The identification 555 for IC 555 timer is mainly because**
    A) It has voltage levels of 5V in the internal circuitry B) It has five Op Amp comparators internally
    C) It has a series of three $5k\Omega$ resistors in the internal circuitry D) None of these
12. **IC 555 timer operating as a free running oscillator is a**
    A) DC to AC converter B) AC to DC converter
    C) DC to DC converter D) DC to DC inverter

6.	a)	Explain the V-I characteristics of SCR with the help of relevant diagrams.	8	L2	3
	b)	With circuit diagrams, derive output voltage of (i) inverting amplifier (ii) inverting adder with 2 inputs.	8	L2	4
	c)	For an IC 555 timer based astable multivibrator given D = 75%, f = 1 kHz, R_2 = 3.6 kΩ, C = 0.1 μF. Calculate T_{ON} and R_1.	4	L2	4

Unit – III

7.	a)	Convert the following number systems (i) $(1076)_8 = (?)_{16}$ (ii) $(724)_8 = (?)_{10}$ (iii) $(9B2.1A)_{16} = (?)_{10}$ (iv) $(10AF)_{16} = (?)_2$	8	L3	5
	b)	Define multiplexer and decoder. Write block diagram and implementation of 2:4 decoder using basic gates and explain.	8	L2	5
	c)	Implement XOR gate and XNOR gate using logic gates.	4	L2	5
8.	a)	Add the following numbers using binary addition method (i) $(84)_{10} + (63)_{10}$ (ii) $(1010111011)_2 + (0111010110)_2$	8	L3	5
	b)	Draw the block diagram of full adder, write the truth table and show the realization using basic gates.	8	L2	5
	c)	With symbol and functional table, explain the operation of D-flipflop.	4	L2	5

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

First Semester B.E. (Credit System) Degree Examinations

April - May 2022

21EC112 – BASIC ELECTRONICS

Max. Marks: 100

ation: 3 Hours

*Note: Answer **Five full** questions choosing **Two full** questions from **Unit – I** & **Unit – II** each and **One full** question from **Unit – III**.*

		Marks	BT*	CO*	PO*
	Unit – I				
a)	Explain the five important diode parameters. Draw the circuit and find the forward current in a circuit consisting of silicon and germanium diodes in series with a 6V battery and 2 kΩ resistor.	8	L*3	1	1
b)	Explain the working of full wave rectifier using two diodes with neat circuit diagram, input and output waveforms. Derive the expressions for V_{DC} and V_{RMS} of the same.	8	L2	1	1
c)	A RC oscillator circuit has an oscillating frequency of 2 kHz. Its feedback circuit has the value of capacitor as 0.3 μF. What must be the value of R in the feedback circuit so that it generates sustained oscillations?	4	L3	2	1
a)	With the help of appropriate diagrams, explain LED and Photo diode.	8	L2	1	1
b)	Describe the phase reversal concept in a single stage RC coupled amplifier with a neat sketch. Draw input and output waveforms.	8	L2	2	1
c)	State and explain Barkhausen's criterion.	4	L2	2	1
a)	In a bridge rectifier,a diode whose internal resistance is 20Ω is used to supply power to a 1000Ω load from 110V (rms) source of supply, calculate (i) DC load current (ii) DC voltage (iii) DC power delivered to the load (iv) efficiency of rectifier	8	L3	1	1
b)	Explain the input and output characteristics of CE configuration with the help of appropriate figures.	8	L2	2	1
c)	In a Hartley oscillator, tank circuit has L_1 =20 μH and L_2 = 2 mH with f = 950 kHz. Calculate the value of capacitor, C.	4	L3	2	1
	Unit – II				
a)	Draw the circuit diagram and drain characteristics of n-channel enhancement MOSFET and explain working of it.	8	L2	3	1
b)	Design an inverting adder circuit using op-amp to obtain the output voltage given by $V_o = 2(0.1\ V_1+0.5\ V_2+2V_3)$ where V_1, V_2 and V_3 are input voltages. Given R_f=10 kΩ.	8	L3	4	1
c)	List any four ideal op-amp characteristics.	4	L1	3	1
a)	Explain the working of inverting and non-inverting comparator with positive reference voltage with neat circuit diagram and waveforms.	8	L2	4	1
b)	Explain the operation of n-channel JFET with circuit diagrams and drain characteristics.	8	L2	3	1
c)	With the circuit diagram, explain the working of CMOS inverter circuit.	4	L2	3	1

P.T.O.

	b)	List the ideal values of each parameter of op-amp.	5	L2	4
	c)	Determine the output voltage of the Op-Amp having differential voltage gain of 4×10^4, CMRR of 40 dB, inverting input voltage of 150 μV and non-inverting input voltage of 140 μV.	5	L3	4
6.	a)	Draw the inverting and non-inverting configurations of op-amp. Explain the operation with input and output waveforms and derive the expressions for voltage gains.	10	L2	4
	b)	Sketch the op-amp circuit for adding three input voltages connected to its inverting terminal. Derive the expression for the output voltage.	5	L2	4
	c)	Show how the 555-timer can be connected as an astable multivibrator. Sketch the output waveform and give the expression for time period.	5	L2	4

Unit – III

7.	a)	Convert the decimal number 1008.75 to hexadecimal, binary and octal number systems.	6	L3	5
	b)	Perform addition of $23_{(10)}$ and $42_{(10)}$ in binary.	4	L3	5
	c)	Simplify Y = (AB' + CD) (B'E + CD) by applying the Boolean theorems.	4	L3	5
	d)	Implement the following Boolean expressions using basic gates. i) $Y = AB + \overline{A}CD + B\overline{C}D + AB\overline{D}$ ii) $A = X\overline{Z} + YX + XY\overline{Z} + X\overline{Y}$ iii) $Y = \overline{A}\overline{B}C + ABD + A\overline{C}D + BC$	6	L3	5
8.	a)	Draw the truth table of full-adder, obtain the simplified expressions for Sum and Carry and realize the same using basic gates.	10	L2	5
	b)	Explain a 4:1 multiplexer by giving its truth table. Realize the same using basic gates.	6	L2	5
	c)	Draw the circuit of gated D-latch using NAND gates and give its truth table.	4	L2	5

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

First / Second Semester B.E. (E&C) (Credit System) Degree Examinations

Supplementary Examination - September 2022

20EC112 / 17EC112 – BASIC ELECTRONICS

uration: 3 Hours | Max. Marks: 100

*Note: 1) Answer **Five full** questions choosing **Two full** questions from **Unit – I** & **Unit – II** each and **One full** question from **Unit – III.***

2) Suitably assume missing data, if any.

		Marks	BT*	CO*	PO*
	Unit – I				
a)	Draw the two-diode full-wave rectifier for getting positive output voltage. Sketch the input and output waveforms and explain the circuit operation along with the expressions for average and RMS output voltages.	10	L*2	1	1
b)	With neat diagrams, explain the construction, operation and characteristics of a photo-diode.	6	L2	1	1
c)	Design a 6.2 V Zener voltage regulator to operate from a 16 V power supply, so as to supply maximum possible load current. Assume $P_{D(max)}$ = 400 mW.	4	L3	1	1
a)	Draw a block diagram of npn BJT. Identify each part and terminal of the device, show the depletion regions, and current directions. Explain the operation when the BJT is biased in active region.	10	L2	2	1
b)	Draw a circuit diagram to show how a BJT can be used as a switch. Show the typical input and output voltages and mention its application.	6	L2	2	1
c)	Calculate α_{dc}, β_{dc} and I_B of a BJT that has I_C = 2.5 mA and I_E = 2.55 mA.	4	L3	2	1
a)	With a neat block diagram, explain the voltage series negative feedback employed in linear amplifiers. List the major advantages and disadvantages of negative feedback on the amplifier performance.	10	L2	2	1
b)	State the Barkhausen criteria for a sinewave oscillator. Explain how they are satisfied by taking the example of RC phase-shift oscillator.	6	L2	2	1
c)	Draw the circuit of Colpitts oscillator using either BJT or Op-amp. If the inductor value is 100 mH, what should be the value of the equivalent capacitance to produce 40 kHz output waveform?	4	L3	2	1
	Unit – II				
a)	Sketch the block schematic of n-channel JFET, showing the bias voltages, depletion regions and current directions. Explain the operation, highlighting the effect of increasing the magnitude of gate-source voltage.	10	L2	3	1
b)	Draw the typical V_{DS}-I_D characteristics of n-channel enhancement MOSFET and explain the same.	5	L2	3	1
c)	Sketch the forward and reverse characteristics of SCR and briefly explain the same.	5	L2	3	1
a)	Explain the following parameters with respect to Op-Amp: (i) CMRR, (ii) Input offset voltage, (iii) Output offset voltage, (iv) Slew rate and (v) Input bias current.	10	L2	4	1

P.T.O.

Unit – II

4.	a)	With neat diagrams explain the construction, operation and drain characteristics of a N channel enhancement type MOSFET.	10	L2	3
	b)	Derive the expression for output voltage of integrator circuit constructed using OPAMP.	6	L2	4
	c)	With neat circuit diagram and waveforms for input and output signal, explain the voltage follower circuit using OPAMP.	4	L2	4
5.	a)	With neat diagrams explain the construction, operation and drain characteristics of a n channel JFET.	10	L2	3
	b)	Explain the working of a OPAMP non - inverting amplifier with neat circuit diagram and waveforms and also derive the expression for A_V.	6	L2	4
	c)	For an N channel JFET, determine I_D for following values of V_{GS} = - 2V and V_{GS} = - 4V. Take I_{DSS} = 8 mA and V_P = - 4V.	4	L3	3
6.	a)	Derive the expressions for the output voltage of an OPAMP circuit in following configurations. Also draw neat diagrams. (i) Inverting amplifier (ii) Differentiator	10	L2	4
	b)	Design an adder circuit using OPAMP to generate an output voltage given by $V_0 = -(2V_1 + 3V_2 + 5V_3)$. Chose R_f = 10 kΩ. Also draw the circuit diagram with components.	6	L3	4
	c)	Explain the operation of N channel JFET as a voltage controlled resistor. Using it's VI characteristics.	4	L2	3

Unit – III

7.	a)	Explain Full adder with truth table and derive expressions for sum and carry. Implement the circuit using basic gates.	10	L2	5
	b)	Realize: (i) Exclusive OR gate using basic gates. Also write the truth table. (ii) $Y = AB + \bar{A}C + BC$ using basic gates.	6	L2	5
	c)	Explain D latch with logic diagram and truth table.	4	L2	5
8.	a)	Perform the following operations: (i) $(615)_8 = (?)_{10}$ (ii) $(CAD.BF)_H = (?)_{10}$ (iii) $(47.8125)_{10} = (?)_2$ (iv) $(FACE)_{16} = (?)_{10}$ (v) $(2AC5.D)_H = (?)_2$	10	L3	5
	b)	Implement the following Boolean expression using logic gates: (i) $Y = (A + \bar{B} + C)(\bar{A} + B + \bar{C})$ (ii) $Y = \bar{A}BC + A\bar{B}C + ABC + AB$	6	L2	5
	c)	Implement Half adder using basic gates. Write the truth table and obtain the expressions for Sum and Carry.	4	L3	5

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

First / Second Semester B.E. (Credit System) Degree Examinations

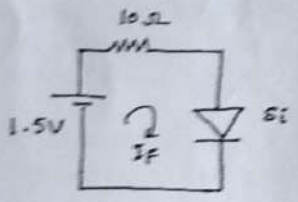
September - October 2022

21EC112 – BASIC ELECTRONICS

Duration: 3 Hours | Max. Marks: 100

*Note: 1) Answer **Five full** questions choosing **Two full** questions from **Unit – I & Unit – II each** and **One full** question from **Unit – III.***

2) Assume missing data suitably.

		Unit – I	Marks	BT*	CO*	PO*
1.	a)	With neat diagram of NPN silicon transistor connected in common emitter configuration, sketch and explain input and output characteristics. Comment on the input and output resistance.	10	L*2	2	1
	b)	Discuss the series voltage negative feedback with neat diagrams and derive the expression for the closed loop gain.	6	L2	2	1
	c)	Explain the application of capacitor filter to reduce ripples in the Half wave rectified signal. Draw relevant waveforms.	4	L2	1	1
2.	a)	With reference to a Full Wave Rectifier: (i) Draw the circuit diagram and explain the operation briefly. (ii) Sketch the waveforms for input ac voltage, load voltage. (iii) Derive the expression for average DC load current and average DC load voltage.	10	L2	1	1
	b)	With neat diagram explain the working of a single stage RC coupled Amplifier. Draw the input and output waveforms. Explain the significance of each component in the circuit.	6	L2	2	1
	c)	Calculate the diode forward current I_F for the diode circuit shown below: 	4	L3	1	2
3.	a)	Explain the operation of Zener voltage regulator with neat circuit diagram. A 5 volt stabilized power supply is required to be produced from a 12 volt DC supply. The maximum power rating of Zener diode is 3 Watts. Calculate: (i) The current through Zener without load (ii) The series resistance (iii) The current through a load resistance of 1 kΩ.	10	L3	1	2
	b)	Explain the construction and working RC phase shift Oscillator with neat diagram.	6	L2	2	1
	c)	In a transistor oscillator L_1 = 10 mH, L_2 = 20 mH and C = 0.01 μF. Calculate: (i) Frequency of oscillations (ii) Feedback factor (iii) Gain required for sustained oscillations	4	L3	2	2

P.T.O.

	c)	Which is the circuit that results when the output of the op-amp is directly connected to the inverting input terminal? Draw the circuit and mention its features and application.	4	L3	4
6.	a)	Sketch the inverting and non-inverting amplifier circuits using op-amp and derive the expressions for their voltage amplification factors.	10	L2	4
	b)	A two-input summing amplifier is to be designed to produce an output of –5V from two 0.25 V inputs. Draw the circuit using IC 741 and calculate the suitable resistor values.	6	L3	4
	c)	A 555-timer pulse wave generator operating from 15 V supply is having R_1 = 390Ω, R_2 = 750Ω and C = 0.5 μF. Calculate the frequency of oscillation.	4	L3	4

Unit – III

7.	a)	Please help a 12th grade CBSE student Yaska to represent the decimal number 1234.56 in binary, octal and hexadecimal number systems, in the shortest possible time with minimum computations.	10	L3	5
	b)	Perform binary addition of i) 24 and 31 ii) 1011101 and 1101011	6	L3	5
	c)	Write the symbol, Boolean expression and truth table of all basic gates.	4	L2	5
8	a)	A binary full-adder circuit is to be designed using only 2-input gates. Draw the truth table, obtain the logic expressions and draw the logic diagram.	10	L3	5
	b)	Construct a D-latch using NAND gates. Explain its operation and write the truth table.	6	L2	5
	c)	A logic circuit connected to two inputs passes one of the two inputs to the output based on the select line. Draw such a circuit using basic gates and show its truth table.	4	L3	5

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester B.E. (Credit System) Degree Examinations

Make up Examination - November 2022

21EC112 - BASIC ELECTRONICS

Duration: 3 Hours | Max. Marks: 100

*Note: 1) Answer **Five full** questions choosing **Two full** questions from **Unit – I** & **Unit – II** each and **One full** question from **Unit – III**.*

2) Suitably assume missing data, if any.

			Marks	BT*	CO*	PO*
		Unit – I				
1.	a)	Sketch the typical forward and reverse characteristics of silicon diode. Explain the characteristics.	10	L*2	1	1
	b)	Draw the Zener voltage regulator circuit with load resistance and explain its operation.	6	L2	1	1
	c)	A halfwave rectifier has a peak voltage of 23V at its secondary. If $R_f = 50\Omega$ and $R_L = 500\Omega$, determine Vdc, Vrms,	4	L3	1	1
2.	a)	Draw the circuit of npn BJT in common base configuration input and output characteristics, clearly labeling the x and y axes with units (no explanation required for the characteristics).	10	L2	2	1
	b)	Discuss the DC load line method used to analyze the transistor circuit in common emitter configuration.	6	L2	2	1
	c)	For a NPN transistor, find I_C and I_E with $\alpha = 0.99$ and $I_B = 20\mu A$.	4	L3	2	1
3.	a)	Using diagram, explain series voltage negative feedback and derive the equation for closed-loop voltage gain.	10	L2	2	1
	b)	Draw the circuit of Colpitt's oscillator, explain its operation and write the equation for frequency of oscillations.	6	L1	2	1
	c)	What is the characteristic feature of the diode fabricated using gallium arsenide phosphide? Briefly explain its operation with symbol.	4	L3	1	1
		Unit – II				
4.	a)	Sketch the structural schematic representation of n-channel JFET showing bias voltages and current directions. Label the device terminals and explain its operation with different levels of gate to source voltage. Also draw the output characteristics.	10	L2	3	1
	b)	Draw the typical drain and transfer characteristics of n-channel enhancement MOSFET and explain briefly.	6	L2	3	1
	c)	What is the name of the device that has two-transistor equivalent circuit? Draw its symbol and characteristics, showing important device parameters.	4	L3	3	1
5.	a)	Draw the circuit symbol and pin diagram of IC 741 op-amp. List any six of its important ideal and typical parameters / characteristics.	10	L2	4	1
	b)	When –0.5 mV is applied to the non-inverting input terminal and +0.5 mV is applied to the inverting input terminal of an op-amp, the output voltage is –8V. When +0.5 mV is applied to both the input terminals, the output is 6 mV. Calculate the CMRR of the op-amp expressed in decibels.	6	L3	4	1

P.T.O.